Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.129”**

**PAD FUNCTIONS:**

1. **V IN**
2. **V OUT**
3. **V OUT**
4. **SENSE**
5. **ADJUST**

**.021”**

**S-D**

**S-D**

**G**

**G**

**.021”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004 X .004” min.**

**Backside Potential: GATE**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .021” X .021” DATE: 1/26/22**

**MFG: InterFET THICKNESS .000” P/N: 2N2609**

**DG 10.1.2**

#### Rev B, 7/1